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Bill,

Here is the abstract front cover page plus machine English translation from JPO.

Regards,

PATENT ABSTRACTS OF JAPAN

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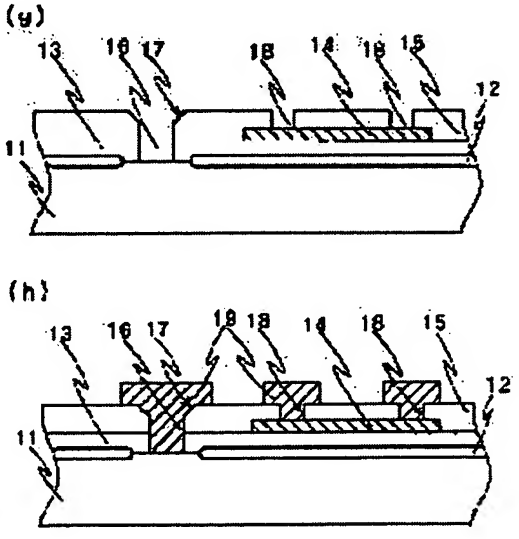
(54) MANUFACTURING METHOD FOR SEMICONDUCTOR INTEGRATED CIRCUIT HAVING THIN FILM RESISTOR

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a manufacturing method for a fine semiconductor integrated circuit having a thin film resistor in which a wiring pattern is formed by dry etching without an additional formation process for a protective film and without needing particular conditions for etching conditions for forming a contact hole.
SOLUTION: An electronic circuit component is formed on a semiconductor substrate 11, and a thin film resistor 14 is formed on a USG film 13 on the surface of the component. A BPSG film (interlayer insulating film) 15 for flattening is formed on the thin film resistor 14 and the USG film 13, and contact holes 16, 18 are formed in the BPSG film and in the USG film for exposing the



connecting portion of the thin film resistor 14 and a portion for connecting the thin film resistor. A wiring material is formed over the entire surface of the substrate thus obtained, and wiring 19 connected with the thin film resistor 14 is formed by patterning by dry etching

LEGAL STATUS

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CLAIMS

[Claim(s)]

[Claim 1] A manufacture method of semiconductor integrated circuit equipment characterized by providing the following of having a thin film resistor A production process which forms an element which constitutes an electronic circuitry in a semiconductor substrate A production process which forms a thin film resistor by forming and carrying out patterning of the thin film for resistors on the 1st insulator layer which does not contain an impurity prepared on the surface of this semiconductor substrate A production process which forms the 2nd insulator layer containing an impurity for flattening on this thin film resistor and said 1st insulator layer A production process which forms a contact hole for exposing this a part of thin film resistor in said 1st and 2nd insulator layers, and a production process which forms wiring connected with said thin film resistor by forming a wiring material on the whole surface and carrying out patterning by dry etching

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] This invention relates to the manufacture method of semiconductor integrated circuit equipment of having a thin film resistor. It is related with the manufacture method of semiconductor integrated circuit equipment of having the thin film resistor which can make a thin film resistor using the almost same production process as the conventional manufacturing process, without increasing a routing counter in more detail, being adapted for detailed-ization accompanying high integration.
[0002]
[Description of the Prior Art] In order to carry out flattening of the USG (undoped silicate glass) film 13 and the surface which are the insulating material which does not contain an impurity on the outcrop of the semiconductor substrate 11 with which the semiconductor device which constitutes an integrated circuit was formed, and field oxide 12 as shown in drawing 4 when making a resistor to a semiconductor integrated circuit for example, a thin film resistor 14 is formed by carrying out the laminating of the BPSG (boro-phospho silicate glass) film 15 which is an insulating material containing an impurity one by one, and forming and carrying out patterning of the thin film resistor material on it. And when connecting the both ends of the thin film resistor 14 to one electrode of the portion which connects electrically, for example, the semiconductor device which formed in the semiconductor substrate 11, in order to expose the electrode, wiring 19 is formed by forming the contact hole 16 in the BPSG film 15 and the USG film 13, forming a wiring material on the whole surface, and carrying out patterning of the wiring material. In addition, since the step coverage of the wiring 19 with an edge is improved in advance of formation of the contact hole 16, PURIETCHI may be performed and the taper section 17 may be formed.
[0003] Although dry etching performs portions other than on a thin film resistor 14 in the case of patterning of this wiring 19, wet etching is performing wiring patterning on a thin film resistor 14. This is because a thin film resistor 14 is damaged and a property is affected in dry etching However, in wet etching, since underetching is carried out to the lower layer of the pattern of wiring 19, while ** which carries out micro processing is not made and being unable to respond to high integration in recent years, in order to have to carry out dry etching and wet etching to patterning of wiring, there is a problem that a manufacturing process becomes complicated.
[0004] In order to solve this problem, for example, as shown in drawing 5 , the method of forming in the surface of a thin film resistor 14 the protective coat 20 which consists of USG(s), such as undoping SiO2, and carrying out patterning of the wiring material by dry etching by once is also used. In addition, the production process to formation of a thin film resistor 14 is formed by repeating membrane formation and patterning like the example shown in above-mentioned drawing 4 .
[0005]
[Problem(s) to be Solved by the Invention] As mentioned above, if a protective coat 20 is formed on a thin film resistor 14 and patterning of the wiring is carried out by dry etching, since exact patterning can be carried out, it can respond to micro processing. However, on a thin film resistor 14, the membrane formation production process which forms a protective coat 20 is needed, and a manufacturing process increases. And since the protective coat 20 prepared in the surface of a thin film resistor 14 makes it as thin as general possible, it is formed in the thickness of about 1000A by it with a USG film. Consequently, since it becomes the three-tiered structure of a USG

film, a BPSG film, and a USG film and etching for contact hole formation differs in the condition by the USG film and the BPSG film, it becomes a very complicated production process and etching conditions must newly be reset up. And as shown in drawing 4 and 5, in order to improve the step coverage of the wiring in a contact hole, in case the contact hole 16 is formed, PURIETCHI is carried out, the taper section 17 is formed, but also in this PURIETCHI, in order to form the taper section 17 in the layer from which a protective coat 20 and the BPSG film 15 differ, new etching conditions must be looked for and there is a problem of becoming a cost rise very much.

[0006] In one side, it sets to a high integration semiconductor device. Surface flattening is indispensable and an impurity like a BPSG film is included as an interlayer insulation film. The insulator layer which does not contain the impurity which prevents that do not obtain a colander using the insulator layer fluidized with heating, and the impurity of a BPSG film is spread in a lower layer semiconductor layer It becomes indispensable to prepare in the lower layer of the insulator layer containing an impurity, and etching conditions for this two-layer structure to always form a line crack and its contact hole in manufacture of semiconductor integrated circuit equipment are also established.

[0007] This invention was made in view of such a condition, and the manufacture process of a thin film resistor is only added between the production processes which form the interlayer insulation film of the two-layer structure in the conventional high integration semiconductor device. With the conditions used for the manufacture method of conventional semiconductor integrated circuit equipment, without adding the formation production process of a protective coat, or making the etching conditions for forming a contact hole into special conditions It aims at offering the manufacture method of detailed semiconductor integrated circuit equipment of having a thin film resistor, forming a circuit pattern by dry etching

[0008]

[Means for Solving the Problem] A manufacture method of semiconductor integrated circuit equipment of having a thin film resistor by this invention A production process which forms a thin film resistor by forming and carrying out patterning of the thin film for resistors on the 1st insulator layer which does not contain a production process which forms an element which constitutes an electronic circuitry in a semiconductor substrate, and an impurity prepared on the surface of this semiconductor substrate, A production process which forms the 2nd insulator layer containing an impurity for flattening on this thin film resistor and said 1st insulator layer, It is characterized by including a production process which forms a contact hole for exposing this a part of thin film resistor in said 1st and 2nd insulator layers, and a production process which forms wiring connected with said thin film resistor by forming a wiring material on the whole surface and carrying out patterning by dry etching

[0009] The conventional contact hole formation conditions can carry out detailed wiring processing only by adding a formation production process of a thin film resistor to a manufacture process of usual semiconductor integrated circuit equipment by using this method, maintaining precision of a thin film resistor highly, since dry etching can perform patterning of wiring, without also giving a damage to a thin film resistor while being able to simplify a manufacture process, since it can carry out by remaining as it is That is, in the usual high integration semiconductor device, surface flattening serves as indispensable conditions and conditions which form a contact hole in an interlayer insulation film of this two-layer structure are also established, using two-layer structure of a BPSG film and a USG film as an interlayer insulation film In this

invention, since a thin film resistor is formed between this USG film and a BPSG film, when carrying out patterning of wiring, even if it does not form specially a protective coat which consists of USG on a thin film resistor, a thin film resistor is protected by BPSG film for flattening, and patterning of precise wiring can be carried out by dry etching

[0010]

[Embodiment of the Invention] Next, the manufacture method of semiconductor integrated circuit equipment of having the thin film resistor of this invention is explained, referring to a drawing. As manufacturing process drawing is shown in drawing 1 -3, the manufacture method of the semiconductor integrated circuit equipment by this invention forms the element which constitutes an electronic circuitry in the semiconductor substrate 11 (drawing 1 (a)), forms the USG film 13 as an interlayer insulation film on the surface of the semiconductor substrate 11 (drawing 1 (b)), and forms a thin film resistor 14 by forming and carrying out patterning of the thin film for resistors on the USG film 13 (drawing 1 (c)). Then, the BPSG film 15 for flattening (interlayer insulation film) is formed on a thin film resistor 14 and the USG film 13 (drawing 2 (d)), and the taper section 17 is formed by making PURIETCHI first the BPSG film 15 of the portion into which the semiconductor layer of the portion linked to a thin film resistor 14 is exposed, and carrying out etching to a longitudinal direction to it (drawing 2 (e)).

[0011] Subsequently, a lengthwise direction is etched, a semiconductor layer is exposed and the contact hole 16 is formed (drawing 2 (f)). Then, in order to expose the connection of a thin film resistor 14, the BPSG film 15 is etched and the contact hole 18 is formed (drawing 3 (g)). And the wiring 19 linked to a thin film resistor 14 is formed by forming a wiring material on the whole surface and carrying out patterning by dry etching

[0012] Next, an example explains to details. First, as shown in drawing 1 (a), a transistor, diode, a diffused resistor, etc. are formed in the semiconductor substrate 11, and an integrated circuit is formed (not shown). Field oxide 12 is formed in the semiconductor substrate 11 surface for isolation.

[0013] and the USG film 13 which becomes the whole surface from SiO2 of undoping etc. as an interlayer insulation film as shown in drawing 1 (b) -- the thickness of about 2000-3000A -- APCVD (atmospheric pressure chemical vapor deposition) -- law or PECVD (plasma enhanced chemical vapor deposition) -- membranes are formed by law.

[0014] Then, as shown in drawing 1 (c), the thin film resistor material which consists of metal tables, such as CrSi, CrSiO, TaSiO, NiCr, TaN, and NbSiO, and a cermet table material on the USG film 13 on field oxide 12 is formed by sputtering. Although the thickness changes with the resistance and materials which are made into the purpose, it serves as dozens - about 1000A of numbers about. When this thin film resistor material film prepares a resist film etc. after forming membranes on the whole surface and patterning is carried out to a desired configuration by etching using photolithography technology, the thin film resistor 14 of a desired configuration is formed.

[0015] below, it is shown in drawing 2 (d) -- as -- a purpose [flattening / surface] -- carrying out -- the BPSG film 15 -- APCVD -- law or PECVD -- law -- about 5000-8000A -- thickness membrane formation is carried out and it heats. In order to perform flattening, a PSG (phospho silicate glass) film besides a BPSG film can be used. In order to fully perform surface flattening, it is desirable to form in the thickness of 5000A or more.

[0016] Next, as shown in drawing 2 (e), PURIETCHI (pre etch) of the BPSG film 15 of contact hole 16 (refer to drawing 2 (f)) portion into which the semiconductor layer of the portion linked

to a thin film resistor is exposed is carried out. This PURIETCHI prevents that the wiring formed in the contact hole 16 is disconnected in the edge portion of a contact hole, and it etches it so that the cross-section configuration of a side wall may become taper-like. In this case, 5000-8000A and since the BPSG film 15 is thick, on the resistor surface, it just needs to etch one kind of interlayer insulation film into the thickness of about 1000A compared with the case where a USG protective coat is formed, and does not need to set up complicated etching conditions.

[0017] Next, as shown in drawing 2 (f), the PURIETCHI portion 17 is etched into a lengthwise direction, and the contact hole 16 is formed. This etching is performed by dry etching.

[0018] Then, as shown in drawing 3 (g), in order to take contact of a thin film resistor 14, it masks and the contact hole 18 is formed similarly.

[0019] Next, as shown in drawing 3 (h), wiring 19 is formed by forming the metal membrane for wiring by sputtering etc., and carrying out and carrying out patterning of the mask. In this case, in order to prevent that the metal of wiring is spread in a lower layer if needed, about 1000A (not shown) of barrier metal layers which consist of TiN, TiW, etc. is formed as a substrate, and about 0.5-1 micrometer of metallic materials, such as aluminum, AlSi, AlSiCu, and AlCu, is formed on it. And patterning is carried out to a predetermined configuration. Under the present circumstances, since the BPSG film 15 is enough and thickness formation is carried out, to dry etching, the resistor film 14 is not damaged or the surface of a thin film resistor 14 is not influenced at all of changing a resistive characteristic etc.

[0020] As mentioned above, when manufacturing the semiconductor integrated circuit equipment which has a thin film resistor according to this invention, the precise circuit pattern by dry etching can be formed only by adding the production process which forms a contact hole also in a thin film resistor, in case the production process which performs membrane formation and patterning of a thin film resistor, and a contact hole are formed between the USG films of an interlayer insulation film and BPSG films which are the usual manufacture process of the semiconductor integrated circuit equipment which does not form a thin film resistor. Namely, since the protective coat which consists of a USG film etc. specially had to be separately formed on the thin film resistor by the conventional method when it was going to form the circuit pattern by dry etching, while a manufacturing process increases Although it is necessary in the case of etching of PURIETCHI for a contact hole or a contact hole to set up new etching conditions since the combination of a USG film and a BPSG film differs from the combination of the usual interlayer insulation film without a thin film resistor According to this invention, the contact hole for the wiring for connecting with the usual interlayer insulation film with a thin film resistor with the process which forms a contact hole can be formed.

[0021] In addition, although the above-mentioned example formed wiring in the semiconductor layer through direct barrier metal When a semiconductor layer and Pt are contacted and a schottky-barrier diode (SBD) is constituted, By forming Pt on the whole surface and performing heat treatment for about 30 minutes at about 400-500 degrees C under nitrogen-gas-atmosphere mind, before forming the contact hole 18 of a thin film resistor 14, after forming the contact hole 16 to which a semiconductor layer is exposed Platinum silicide can also be formed only in the contact section of a semiconductor layer by removing Pt except having formed and silicide-ized platinum silicide ($PtSi_2$) using the mixed liquor (aqua regia) of HCl and HNO_3. In addition, not only platinum silicide but other silicide can be formed, and the electric contact to a semiconductor layer and wiring can also be raised.

[0022]

[Effect of the Invention] As mentioned above, dry etching can perform patterning of wiring by micro processing, without receiving effect in the property of a thin film resistor only by adding the formation production process of a thin film resistor, without replacing most manufacturing processes of conventional semiconductor integrated circuit equipment with according to this invention. Consequently, the semiconductor integrated circuit equipment which has the thin film resistor of a precise property can be obtained very cheaply, corresponding to high integration in recent years.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is explanatory drawing showing the manufacturing process of 1 operation gestalt of the manufacture method by this invention.

[Drawing 2] It is explanatory drawing showing the manufacturing process of 1 operation gestalt of the manufacture method by this invention.

[Drawing 3] It is explanatory drawing showing the manufacturing process of 1 operation gestalt of the manufacture method by this invention.

[Drawing 4] It is cross-section explanatory drawing showing an example of a semiconductor device which has the conventional thin film resistor.

[Drawing 5] It is cross-section explanatory drawing showing other examples of the semiconductor device which has the conventional thin film resistor.

[Description of Notations]

11 Semiconductor Substrate
13 USG Film
14 Thin Film Resistor
15 BPSG Film
16 Contact Hole
18 Contact Hole
19 Wiring

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Subject: BUR8-2003-0491

Abdi, The Search Report for this disclosure lists a Japanese reference as related art: JP2003338549 (Publication date of 2003-11-28). The Japanese text was sent to us, but there was no English title or

abstract. In view of the drawings, the inventors would like to make a close review of the reference. Can you obtain a computerized translation of the text --- This would provide enough info. for our review. Pls. let us know the time frame for obtaining the translation. Thx.

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